CLAIMS

1. A ferroelectric integrated circuit memory comprising:

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film, and a top electrode;

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes.

2. A ferroelectric integrated circuit memory as in claim 1 wherein said ferroelectric film has a thickness not exceeding 80 nm.

3. A ferroelectric integrated circuit memory as in claim 1 wherein said ferroelectric film has a thickness not exceeding 60 nm.

4. A ferroelectric integrated circuit memory as in claim 1 wherein said ferroelectric film comprises ferroelectric layered superlattice material.

5. A ferroelectric integrated circuit memory as in claim 4 wherein said ferroelectric film comprises strontium bismuth tantalate.

6. A ferroelectric integrated circuit memory as in claim 1 wherein said capacitor laminate has a thickness not exceeding 300 nm.

7. A ferroelectric integrated circuit memory as in claim 1 wherein said capacitor laminate has a thickness not exceeding 200 nm.

8. A ferroelectric integrated circuit memory as in claim 1 wherein said laminate defines a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

9. A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

10. A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

11. A ferroelectric integrated circuit memory as in claim 8 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

12. A ferroelectric integrated circuit memory as in claim 8 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

13. A ferroelectric integrated circuit memory as in claim 8 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

14. A ferroelectric integrated circuit memory as in claim 1, comprising a

plurality of capacitor laminates.

15. A ferroelectric integrated circuit memory as in claim 1 wherein said bottom electrode, said ferroelectric film, and said top electrode conform substantially to said 3-D shape.

16. A ferroelectric integrated circuit memory as in claim 1, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

17. A ferroelectric integrated circuit memory as in claim 1, further including a trench formed in a portion of said integrated circuit, and wherein said 3-D capacitor laminate is formed in said trench.

18. A ferroelectric integrated circuit memory as in claim 17, further comprising:

an insulator layer having an insulator top surface, and

wherein said trench is located substantially in said insulator layer, said trench having a trench bottom, a trench sidewall, and a trench opening substantially coplanar with said insulator top surface;

said bottom electrode substantially conforms to said trench bottom and said trench sidewall;

said ferroelectric film is disposed above said bottom electrode layer and substantially conforms to said bottom electrode; and

said top electrode is disposed above said ferroelectric film and substantially conforms to said ferroelectric film.

19. A ferroelectric integrated circuit memory as in claim 17 wherein said ferroelectric film has a thickness not exceeding 60 nm.

20. A ferroelectric integrated circuit memory as in claim 17 wherein said ferroelectric film comprises ferroelectric layered superlattice material.

21. A ferroelectric integrated circuit memory as in claim 17 wherein said bottom electrode, said ferroelectric film, and said top electrode define a capacitance area and a capacitor-footprint area, and said capacitance area is at least two times greater than said capacitor-footprint area.

22. A ferroelectric integrated circuit memory as in claim 21 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

23. A ferroelectric integrated circuit memory as in claim 22 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

24. A ferroelectric integrated circuit memory as in claim 21 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

25. A ferroelectric integrated circuit memory as in claim 24 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

26. A ferroelectric integrated circuit memory as in claim 18 wherein:

said 3-D capacitor laminate has a laminate thickness and a top laminate surface; and

wherein said insulator top surface and said trench bottom define a trench depth; and

wherein said laminate thickness is less than said trench depth.

27. A ferroelectric integrated circuit memory as in claim 26 wherein said laminate thickness does not exceed 300 nm.

28. A ferroelectric integrated circuit memory as in claim 26 wherein said laminate thickness does not exceed 200 nm.

29. A ferroelectric integrated circuit memory as in claim 26 wherein said trench opening has a trench opening area and said top laminate surface has a laminate area, said laminate area being greater than said trench opening area.

30. A ferroelectric integrated circuit memory as in claim 29 wherein laminate area is more than two times greater than said trench opening area.

31. A ferroelectric integrated circuit memory as in claim 29 wherein said trench opening area does not exceed 0.5 nm^2.

32. A ferroelectric integrated circuit memory as in claim 29 wherein said trench opening area does not exceed 0.2 nm^2.

33. A ferroelectric integrated circuit memory as in claim 17, comprising a plurality of trenches and a plurality of corresponding capacitor laminates.

34. A ferroelectric integrated circuit memory as in claim 33 wherein a distance between two adjacent trenches does not exceed 250 nm.

35. A ferroelectric integrated circuit memory as in claim 17, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

36. A ferroelectric integrated circuit memory as in claim 1, further including a pillar formed in a portion of said integrated circuit, and wherein said 3-D capacitor laminate is formed on said pillar.

37. A ferroelectric integrated circuit memory as in claim 36 wherein:

said pillar is formed of insulating material, said pillar having a pillar top surface and a pillar sidewall;

said bottom electrode covers a portion of said pillar, said bottom electrode substantially conforming to said pillar top surface and to a portion of said pillar sidewall;

said ferroelectric film is disposed above said bottom electrode layer, said ferroelectric film substantially conforming to said bottom electrode; and

said top electrode is disposed above said ferroelectric film, said top electrode substantially conforming to said ferroelectric film.

38. A ferroelectric integrated circuit memory as in claim 38 wherein said ferroelectric film has a thickness is not exceeding 60 nm.

39. A ferroelectric integrated circuit memory as in claim 38 wherein said ferroelectric film comprises ferroelectric layered superlattice material.

40. A ferroelectric integrated circuit memory as in claim 38 wherein said bottom electrode, said ferroelectric film, and said top electrode define a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

41. A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

42. A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

43. A ferroelectric integrated circuit memory as in claim 40 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

44. A ferroelectric integrated circuit memory as in claim 40 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

45. A ferroelectric integrated circuit memory as in claim 40 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

46. A ferroelectric integrated circuit memory as in claim 36 wherein:

said 3-D capacitor laminate has a laminate thickness and a top laminate surface; and

wherein said pillar sidewall defines a pillar height; and

wherein said laminate thickness is less than said pillar height.

47. A ferroelectric integrated circuit memory as in claim 46 wherein said laminate thickness does not exceed 300 nm.

48. A ferroelectric integrated circuit memory as in claim 46 wherein said laminate thickness does not exceed 200 nm.

49. A ferroelectric integrated circuit memory as in claim 46 wherein said pillar top surface has a pillar top area and said top laminate surface has a laminate area, said laminate area being greater than said pillar top area.

50. A ferroelectric integrated circuit memory as in claim 49 wherein laminate area is more than two times greater than said pillar top area.

51. A ferroelectric integrated circuit memory as in claim 49 wherein said pillar top area does not exceed 0.5 nm^2.

52. A ferroelectric integrated circuit memory as in claim 49 wherein said pillar top area does not exceed 0.2 nm^2.

53. A ferroelectric integrated circuit memory as in claim 36, comprising a plurality of pillars and a plurality of corresponding capacitor laminates.

54. A ferroelectric integrated circuit memory as in claim 53 wherein a distance between two adjacent pillars does not exceed 250 nm.

55. A ferroelectric integrated circuit memory as in claim 36, further comprising a nonconductive hydrogen barrier layer disposed above said capacitor laminate, said nonconductive hydrogen barrier layer comprising strontium tantalate.

56. A method of forming a ferroelectric memory in an integrated circuit substrate, comprising:

providing an integrated circuit substrate including a bottom electrode having a three-dimensional (3-D) shape having substantial directional components in three mutually orthogonal planes;

placing said integrated circuit substrate in a chemical vapor deposition chamber;

depositing a conformal ferroelectric thin film on said bottom electrode using a

chemical vapor deposition process; and

depositing a conformal top electrode layer conforming to said ferroelectric thin film layer.

57. A method as in claim 56 wherein said integrated circuit substrate includes an insulator layer, a portion of which insulator layer forms a three-dimensional ("3-D") insulator surface, and said providing comprises depositing said bottom electrode layer conforming to said 3-D insulator surface.

58. A method as in claim 57 wherein said integrated circuit substrate includes a switch and said insulator layer is formed above said switch.

59. A method as in claim 56, further comprising processes of removing a portion of said top electrode layer, a portion of said ferroelectric thin film layer, and a portion of said bottom electrode layer to form a 3-D capacitor laminate including a top electrode, a ferroelectric film and a bottom electrode.

60. A method as in claim 56 wherein said depositing a conformal ferroelectric thin film layer comprises depositing a ferroelectric thin film layer having a thickness not exceeding 80 nm.

61. A method as in claim 56 wherein said depositing a conformal ferroelectric thin film layer comprises depositing a ferroelectric thin film layer having a thickness not exceeding 60 nm.

62. A method as in claim 56 wherein said depositing a conformal ferroelectric thin film layer is conducted using a low-thermal-budget MOCVD technique.

63. A method as in claim 59 wherein said using a MOCVD technique comprises:

flowing a metal organic precursor into a MOCVD reaction chamber containing said integrated circuit substrate to form a coating on said conformal bottom electrode layer, said precursor containing metal atoms in effective amounts for forming said ferroelectric thin film layer; and

heating said substrate including said coating using rapid thermal processing at a temperature in a range of about from 500°C to 900°C for a cumulative heating time not exceeding 30 minutes.

64. A method as in claim 63, further characterized in which said cumulative

heating time does not exceed five minutes.

65. A method as in claim 63, further characterized by not heating said substrate in a furnace.

66. A method as in claim 63 wherein said heating said substrate comprises:

conducting a pre-TE RTP treatment of said substrate including said coating before said depositing said top electrode layer; and

wherein said heating said substrate further comprises conducting a post-TE RTP treatment after said depositing said top electrode layer.

67. A method as in claim 66, further comprising processes of removing a portion of said top electrode layer, a portion of said ferroelectric thin film layer, and a portion of said bottom electrode layer to form a 3-D capacitor laminate including a top electrode, a ferroelectric film, and a bottom electrode before conducting said post-TE RTP treatment.

68. A method as in claim 66 wherein said conducting said post-TE RTP treatment is done in a nonreactive gas.

69. A method as in claim 56 wherein said depositing comprises depositing a layered superlattice material.

70. A ferroelectric integrated circuit memory comprising:

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film comprising a layered superlattice material, and a top electrode; and

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes.

71. A ferroelectric integrated circuit memory as in claim 70 wherein said layered superlattice material comprised a material selected from the group consisting of strontium bismuth tantalate, strontium bismuth tantalum niobate, and bismuth lanthanum titanate.

72. A ferroelectric integrated circuit memory comprising:

a three-dimensional ("3-D") capacitor laminate, said capacitor laminate comprising a bottom electrode, a ferroelectric film, and a top electrode;

wherein said 3-D capacitor laminate comprises a 3-D shape having substantial directional components in three mutually orthogonal planes; and

wherein said capacitor laminate has a thickness not exceeding 300 nm.

73. A ferroelectric integrated circuit memory as in claim 72 wherein said capacitor laminate has a thickness not exceeding 200 nm.

74. A ferroelectric integrated circuit memory as in claim 72 wherein said laminate defines a capacitance area and a capacitor-footprint area, and said capacitance area exceeds said capacitor-footprint area.

75. A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least two times greater than said capacitor-footprint area.

76. A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least three times greater than said capacitor-footprint area.

77. A ferroelectric integrated circuit memory as in claim 74 wherein said capacitance area is at least four times greater than said capacitor-footprint area.

78. A ferroelectric integrated circuit memory as in claim 74 wherein said capacitor-footprint area does not exceed 0.5 nm^2.

79. A ferroelectric integrated circuit memory as in claim 74 wherein said capacitor-footprint area does not exceed 0.2 nm^2.

80. A ferroelectric integrated circuit memory as in claim 72 wherein said ferroelectric film has a thickness not exceeding 80 nm.

81. A ferroelectric integrated circuit memory as in claim 72 wherein said ferroelectric film has a thickness not exceeding 60 nm.